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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/552,364	06/09/2006	Christopher Julian Travis	GRP-0142	8785

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EXAMINER	
GANNON, LEVI	

ART UNIT	PAPER NUMBER
2817	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

TH

Office Action Summary	Application No.	Applicant(s)	
	10/552,364	TRAVIS, CHRISTOPHER JULIAN	
	Examiner	Art Unit	
	Levi Gannon	2817	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 September 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-90* is/are pending in the application.

4a) Of the above claim(s) *23-54 and 59-85* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22,55-58 and 87-90* is/are rejected.

7)☒ Claim(s) *86* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *10/3/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election without traverse of Invention I, Claims 1-22, 55-58, and 86-90 in the reply filed on 9/06/07 is acknowledged.

Claim Objections

Claim 86 is objected to under 37 CFR 1.75(c) as being in improper form because a multiple dependent claim should refer to other claims in the alternative only. See MPEP § 608.01(n). Accordingly, the claim has not been further treated on the merits.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-6, 9, 10, 12-22, 55-58, and 87-90 are rejected under 35 U.S.C. 102(e) as being anticipated by Wunner et al. (hereinafter "Wunner") (US Patent 6,674,332).

Regarding claim 1, Wunner discloses a method (Note figures 4 and 5 for reference.) of establishing an output clock signal (output of 533 and 212E in figure 5) on a basis of an input timing reference (Input Ref 205), said method comprising: attenuating jitter (using loop filter 432) of said input timing reference to produce a control

signal (216"), providing at least one intermediate clock signal (213 and output of divider 212C) on a basis of said control signal, at least one of said intermediate clock signals (213 and output of divider 212C) being justified to a local clock (provided by crystal 242) and being spectrum controlled (note column 7, lines 31-36), and providing said output clock signal (output of 533 and 212E in figure 5) on a basis of said at least one intermediate clock signal (213 and output of divider 212C) by attenuating jitter (using loop filter 532) of said at least one intermediate clock signal (213 and output of divider 212C).

In terms of claim 2, Wunner teaches at least a part of the jitter of said at least one intermediate clock signal (213 and output of divider 212C) comprises justification jitter originating from said justification to said local clock (provided by crystal 242).

As for claim 3, Wunner teaches the justification and spectrum control being performed numerically (By way of controlling oscillator 232" frequency and divider 212C).

As for claim 4, Wunner teaches the attenuation of jitter of said input timing reference (205) being performed by using low-pass filtering (in filter 432).

In terms of claim 5, Wunner teaches the justification being performed by means of a number-controlled oscillator (comprising oscillator 232" and frequency divider 212C).

Regarding claim 6, Wunner a control input (f216") of said number-controlled oscillator (comprising oscillator 232" and frequency divider 212C) comprises a period control input.

As for claims 9 and 10, Wunner teaches the local clock being derived from a stable crystal reference clock (242).

Regarding claim 12, Wunner discloses the attenuation of jitter of said input timing reference (205) is performed by means of a first block (figure 4), which preferably comprises a time-locked loop (see figure 4), with reference to a stable reference clock (crystal 242).

As for claim 13, Wunner teaches at least a part of said justification jitter (derived by oscillator 232" and divider 212C) being biased into a higher frequency band (jitter may be biased into whatever frequency band is determined by oscillator 232" and divider 212C).

In terms of claim 14, Wunner discloses the justification jitter being low-pass filtered by means of a second block (figure 5), which preferably comprises a phase-locked loop (note figure 5).

As for claim 15, Wunner teaches the second block (figure) producing a multiplied clock (output of 533).

Regarding claim 16, Wunner teaches the second block (figure 5) further produces a frame signal (210), said frame signal (210) being established by means of frequency division (with 212E) of said multiplied clock (output of 533).

Regarding claim 17, Wunner teaches intermediate clock signals (213 and output of 212C) is established by means of at least one numeric stage (figure 4).

As for claim 18, Wunner teaches the attenuating jitter of said at least one intermediate clock signal (213 and output of 212C) is performed by means of at least one analog stage (figure 5).

In terms of claim 19, Wunner teaches the analog stage (figure 5) is adapted for attenuating jitter partly or mainly originating from said at least one numeric stage (figure 4).

As for claim 20, Wunner discloses the intermediate clock signals (IC) being justified to a corresponding local clock (from crystal 242) and justification jitter associated with said justification to said local clock is spectrum controlled (with chosen frequency of oscillator 232" and frequency divider 212C).

As for claim 21, Wunner teaches the intermediate clock signals (213 and output of 212C) comprising an intermediate event clock component (213) and an intermediate framing component (output of 212C), said intermediate framing being established on a basis of said intermediate event clock by means of frequency division (with 212C).

In terms of claim 22, Wunner discloses the output clock signal (210 and output of 533) comprises an output event clock component (output of 533) and an output framing component (210), said output framing being established on the basis of said output event clock by means of frequency division (with 212E).

In terms of claim 55, Wunner teaches a clock synchronizer (Wunner synchronizes input 205 and output 210) for establishment of an output clock signal (210 and output of 533) according to claim 1.

As for claim 56, Wunner teaches a number-controlled oscillator (comprising oscillator 232" and frequency divider 212C).

In terms of claim 57, Wunner discloses a circuit (figure 4) for attenuating jitter of an input timing reference (205), said circuit comprising a number-controlled oscillator (comprising oscillator 232" and frequency divider 212C) adapted for establishment of an intermediate clock signal (213 and output of 212C) on the basis of said input timing reference (205).

Regarding claim 58, Wunner teaches jitter filtering means (figure 5) adapted for providing said output clock signal (210 and output of 533) on the basis of said intermediate clock signal (213 and output of 212C).

As for claim 87, Wunner teaches the second block (figure 5) comprising an asynchrony detector (531).

In terms of claims 88-90, Wunner teaches the output clock signal (210 and output of 533) being phase, frequency, and frequency ratio locked to the input timing reference (205).

Claims 1 and 11 are rejected under 35 U.S.C. 102(b) as being anticipated by Wang (US Patent 6,094,569).

Regarding claim 1, Wang discloses a method of establishing an output clock signal (output of VCO2) on a basis of an input timing reference (fref), said method comprising: attenuating jitter (using LF1) of said input timing reference (fref) to produce a control signal (output of LF1), providing at least one intermediate clock signal (output

of VCO1 and divider 34) on a basis of said control signal, at least one of said intermediate clock signals (output of VCO1 and divider 34) being justified to a local clock (from VCO2) and being spectrum controlled (By setting frequency of VCO1 and setting the value of M in divider 34), and providing said output clock signal (output of VCO2) on a basis of said at least one intermediate clock signal (output of VCO1 and divider 34) by attenuating jitter (using LF2) of said at least one intermediate clock signal (output of VCO1 and divider 34).

In terms of claim 11, Wang teaches the local clock (from VCO2) being derived from said output clock signal (from VCO2).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wunner.

Regarding claims 7 and 8, Wunner teaches the method of establishing an output clock signal according to claim 1, as stated above, but fails to expressly teach the spectrum control comprising dithering or noise shaping.

However, applying dithering and noise shaping to a frequency divider of a phase locked loop in order to provide spectrum control are well known techniques of spectrum control to those of ordinary skill in the art.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the invention to provide dithering or noise shaping to the phase locked loop of Wunner (figures 4 and 5) in order to provide spectrum control to the phase locked loop of Wunner because such modification would have merely been making use of well known spectrum control techniques.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following US Patents teach establishing output clocks using at least a timing reference, a local clock, an intermediate clock, attenuation, and frequency dividers: 6,833,764, 6,611,175, and 4,970,474.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Levi Gannon whose telephone number is (571) 272-7971. The examiner can normally be reached on Monday-Friday 9:30AM-6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal can be reached on (571) 272-1769. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

LG

Robert J. Pascal
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